AMENDMENTS TO THE CLAIMS

The following is a complete, marked up listing of the claims with underlined text indicating insertions, strikethrough and/or double-bracketed text indicating deletions, and a parenthetical indicator reflecting the status of each of the listed claims.

LISTING OF CLAIMS

1. (ORIGINAL) A semiconductor package, comprising:

a board having an upper surface, a lower surface and an aperture;

a plurality of solder bump pads formed on the lower surface of the board;

a plurality of board pads formed on the lower surface of the board;

a plurality of distribution patterns for electrically connecting the solder bump pads to the board pads;

a plurality of contact pads formed on the upper surface of the board, and electrically connected to the solder bump pads;

at least one chip having a plurality of bonding pads, disposed in the aperture;

a plurality of bonding wires electrically connecting the bonding pads to the board pads, at least one end of the bonding wires being bonded to the bonding pads or the board pads by wedge bonding;

an encapsulation part provided on the lower surface of the board for encapsulating the at least one chip, the plurality of bonding wires and the plurality of board pads; and

a plurality of solder bumps formed on the plurality of solder bump pads.

2. (ORIGINAL) The semiconductor package according to claim 1,

wherein the height of each solder bump is greater than the height of the encapsulation part extending over the lower surface of the board.

3. (ORIGINAL) The semiconductor package according to claim 1,

wherein the board is covered with a solder resist except for the regions above the plurality of solder bump pads, the plurality of contact pads and the plurality of board pads.

4. (ORIGINAL) The semiconductor package according to claim 1, further comprising:

a plurality of via holes formed through the board for electrically connecting the solder bump pads to the contact pads.

5. (ORIGINAL) A package stack including a plurality of the semiconductor packages according to claim 1,

wherein at least one solder bump of an upper package of any two adjacent packages is electrically connected to at least one contact pad of the lower package of the two adjacent packages.

6. (CURRENTLY AMENDED) A method of manufacturing a semiconductor package, comprising:

forming a plurality of solder bump pads on one surface of a board;

forming a plurality of board pads on the one surface of the board;

placing at least one chip having a plurality of bonding pads in an aperture of the board;

forming a plurality of contact pads on a surface of the board opposite the one surface of the board, the plurality of contact pads being electrically connected to corresponding ones of the plurality of solder bump pads;

wedge bonding at least one end of a plurality of bonding wires to electrically connect the bonding pads to the plurality of board pads;

encapsulating the at least one chip, the plurality of bonding wires and the plurality of board pads on the one surface of the board; and

forming a plurality of solder bumps on the plurality of solder bump pads.

7. (ORIGINAL) The method of claim 6,

wherein the height of each solder bump is greater than the height of the encapsulation part extending over the one surface of the board.

8. (ORIGINAL) The method of claim 6, wherein at least one solder bump of an upper package of any two adjacent packages is electrically connected to at least one contact pad of the lower package of the two adjacent packages.

9. (ORIGINAL) The method of claim 6, wherein the semiconductor package includes

the board having an upper surface, a lower surface and the aperture;

the plurality of solder bump pads formed on the lower surface of the board;

the plurality of board pads formed on the lower surface of the board;

the plurality of distribution patterns for electrically connecting the solder bump pads to the board pads;

the plurality of contact pads formed on the upper surface of the board, and electrically connected to the solder bump pads;

the at least one chip having the plurality of bonding pads, disposed in the aperture;

the plurality of bonding wires electrically connecting the bonding pads to the board pads;

the encapsulation part provided on the lower surface of the board for encapsulating the at least one chip, the plurality of bonding wires and the plurality of board pads; and

the plurality of solder bumps formed on the plurality of solder bump pads.

10. (NEW) A method of manufacturing a semiconductor package, comprising:

forming a board having an upper surface, a lower surface and an aperture;

forming a plurality of solder bump pads on the lower surface of the board;

forming a plurality of board pads on the lower surface of the board;

placing a semiconductor chip in the aperture, the semiconductor chip having a plurality of bonding pads arrayed on an active surface and the aperture being sized to expose substantially all of the active surface;

forming a plurality of contact pads on the upper surface of the board, the contact pads being electrically connected to corresponding ones of the solder bump pads;

wedge bonding at least one end of a plurality of bonding wires to electrically connect the bonding pads to the plurality of board pads;

encapsulating the active surface of semiconductor chip, the bonding pads, the bonding wires and the board pads; and

forming a plurality of solder bumps on the plurality of solder bump pads.

11. (NEW) A method of manufacturing a semiconductor package according to claim 10, wherein:

the bonding pads are arranged in a double row configuration.

12. (NEW) A method of manufacturing a semiconductor package according to claim 11, wherein:

each of the rows of bonding pads are positioned in peripheral regions of the active surface.

13. (NEW) A method of manufacturing a semiconductor package according to claim 10, further comprising:

forming a plurality of connective vias through the board to provide electrical contact between the contact pads and the corresponding ones of the solder bump pads.

14. (NEW) A method of manufacturing a semiconductor package according to claim 10, further comprising:

forming an insulating layer on a peripheral portion of the lower surface of the board;

wherein the bonding wires are configured to remain below a plane defined by an exposed surface of the insulating layer.

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